Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A trench-capacitor DRAM cell, comprising:

an active area island comprising a horizontal surface and a vertical surface;

a pass transistor comprising a folded gate conductor extending from the horizontal surface of the active area island to the vertical surface, a source doped region situated in the horizontal surface of the active area island, and a drain doped region situated in the vertical surface of the active area island; and

a trench capacitor formed below the folded gate conductor and isolated from the folded gate conductor with an insulation layer, the trench capacitor being electrically connected to the pass transistor through the drain doped region.

[c2] 2.The trench-capacitor DRAM cell of claim 1 wherein the folded gate conductor on the vertical surface of the active area island is covered by a dielectric layer.

[c3] 3.The trench-capacitor DRAM cell of claim 2 wherein the dielectric layer is a high-density plasma CVD (HDPCVD) silicon oxide layer.

[c4] 4.The trench-capacitor DRAM cell of claim 2 wherein the dielectric layer is substantially coplanar with a top surface of the folded gate conductor on the horizontal surface of the active area island.

[c5] 5.The trench-capacitor DRAM cell of claim 1 wherein the folded gate conductor comprises a polysilicon layer and a silicon nitride cap layer.

[c6] 6.The trench-capacitor DRAM cell of claim 1 wherein the folded gate conductor further extends from the vertical surface of the active area island to a top surface of the insulation layer.

[c7] 7.The trench-capacitor DRAM cell of claim 1 wherein the insulation layer is made of HDPCVD oxide.

[c8] 8.The trench-capacitor DRAM cell of claim 1 wherein the insulation layer is a trench top oxide (TTO) layer.

[c9] 9.The trench-capacitor DRAM cell of claim 1 wherein the pass transistor further comprises a gate oxide layer disposed underneath the folded gate conductor.